Project ID:ELT238 Award No:DE-EE0008450

Intelligent, Grid-Friendly, Modular Extreme Fast Charging System with Solid-State Direct-Current Protection

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ABB FREEDM SYSTEMS CENTER NEW YORK STATE OF OPPORTUNITY NY Power Authority NC STATE UNIVERSITY

Overview

Timeline

- Project Start Date: Oct. 2018
- Project End Date: July 2022
- Percent Complete: 20%

Budget

- Total Project Funding
  - DOE Share: $ 2,675,952
  - Contractor Share: $ 3,323,775
- Funding for 2020
  - DOE Share: $ 1,099,164
  - Contractor Share: $ 1,336,347

Barriers

- Integration to utility at medium voltage
- Protection
- System siting, integration and deployment

Partners

- NCSU/FREEDM – Lead
- ABB Inc.
- New York Power Authority (NYPA)

Relevance

Objectives:

- Develop an electric vehicle (EV) extreme fast charging (XFC) station with direct connection to the medium voltage distribution network
- Develop a direct-current (DC) distribution network with solid-state protection to supply multiple EV charging ports

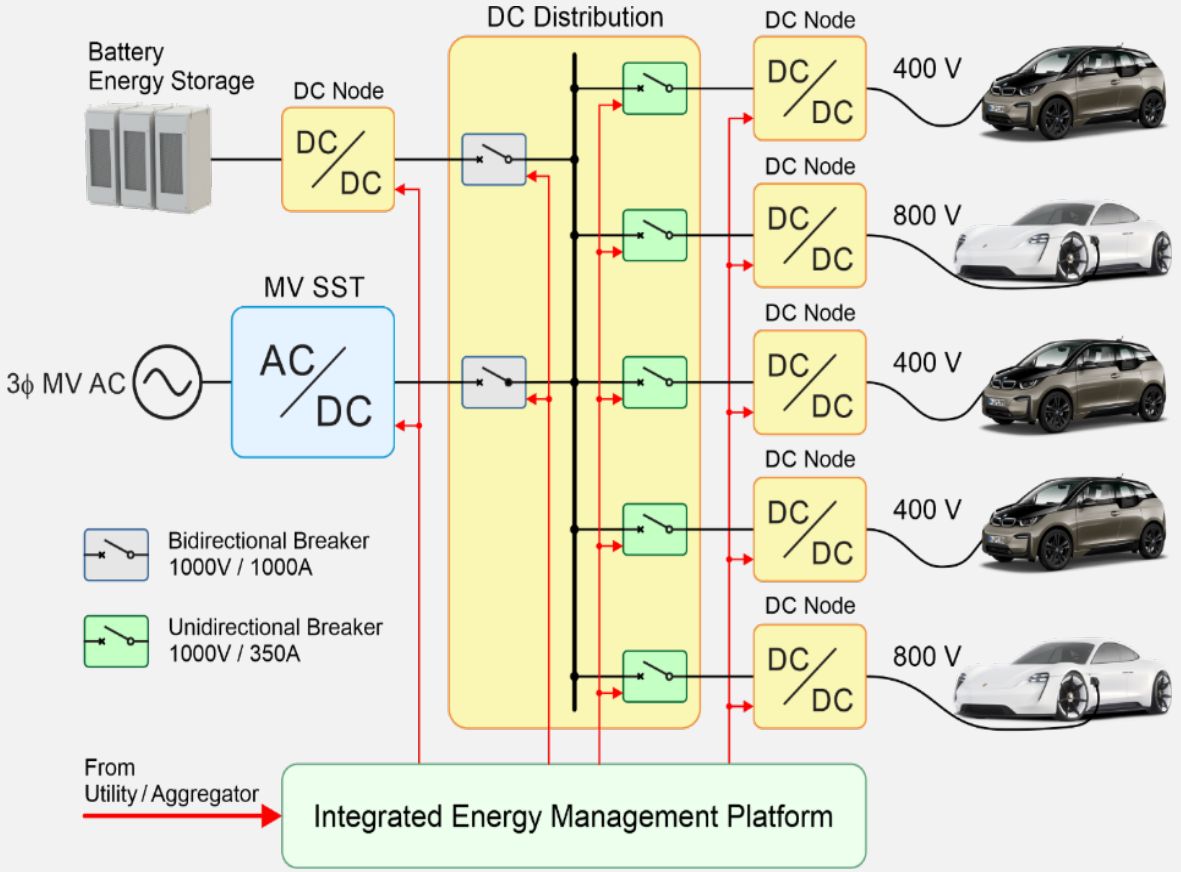
Project Impact:

- Framework for designing XFC stations to minimize installation and operating costs, manage grid impact, and provide design flexibility
- Field demonstration of novel technologies for future XFC installations
- Installation, operation and maintenance guidelines for deployment of XFC infrastructure with proposed unique architecture.

Approach

Develop and deploy a 1 MW medium voltage XFC station:

- Shared bi-directional Solid State Transformer (SST) connecting directly to the medium voltage (MV) distribution system
- DC distribution network with solid-state DC protection
- Energy management platform
- DC Nodes for local isolation and DC/DC conversion



Milestones

BP1 — System Development

- **Construct SST & DC node***
- Select site
- Preliminary engineering diagrams
- SST & DC nodes operational
- Engineering diagrams complete

10/1/2018 – 7/31/2020

BP2 — System Integration

- **Complete system integration ***
- Site preparation complete
- System integration
- Protection validated
- Safety evaluation

8/1/2020 – 7/31/2021

BP3 — System Deployment

- **Commission System**
- System transported and installed
- Use cases tested
- Data collection
- Public demonstration

8/1/2021 – 7/31/2022

* Denotes Go/No-Go Milestone

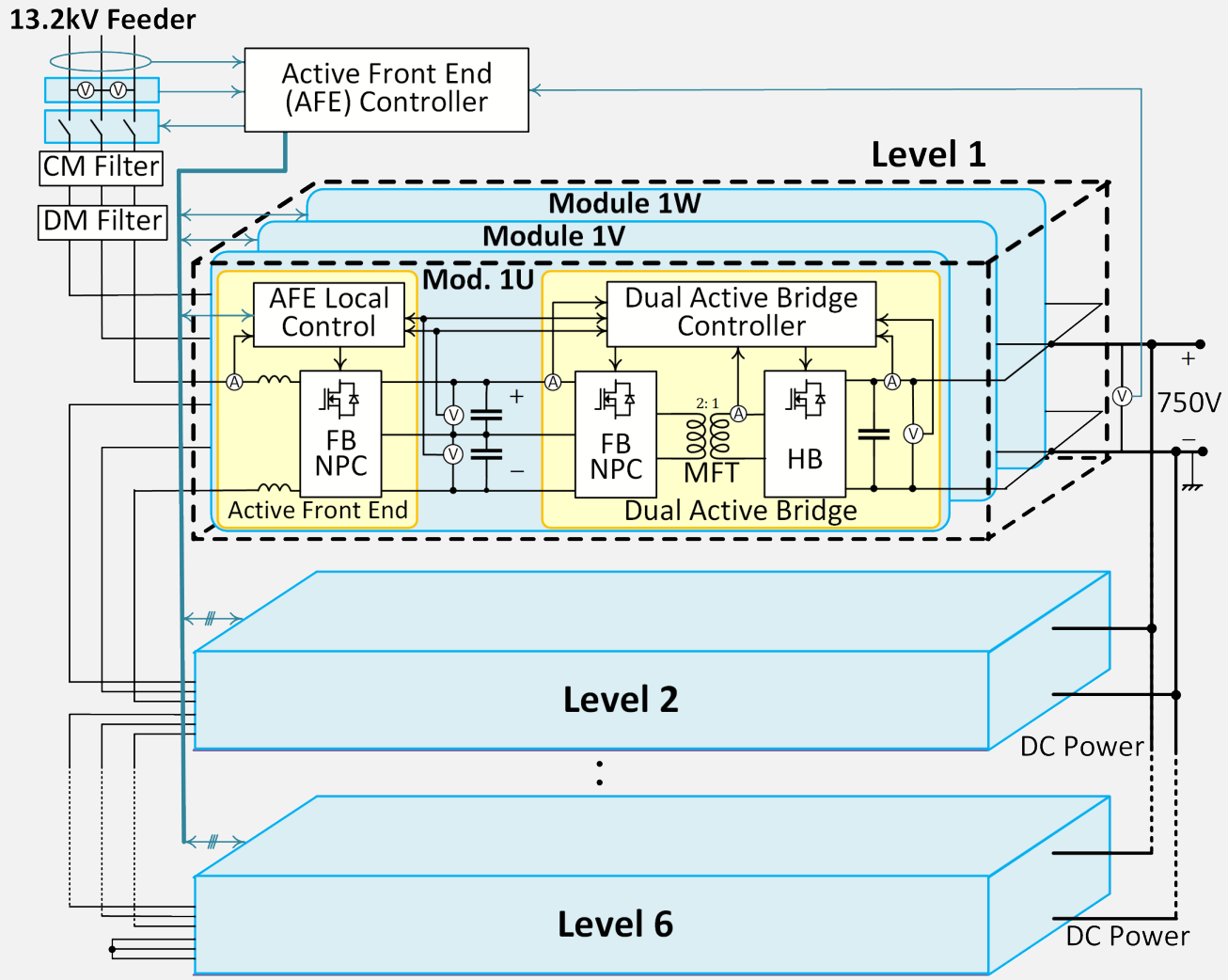
BP: Budget Period

Technical Accomplishments & Progress

- Deployment Site Selected
- Solid State Transformer (SST) design and control approach finalized and validated
- System simulation model built, analysis completed, module performance at system level evaluated
- SST Module Constructed and Tested
- DC Solid State Breakers constructed; developed EV charging infrastructure protection coordination
- Leveraged proven, near-commercial ABB product line to de-risk DC Node development

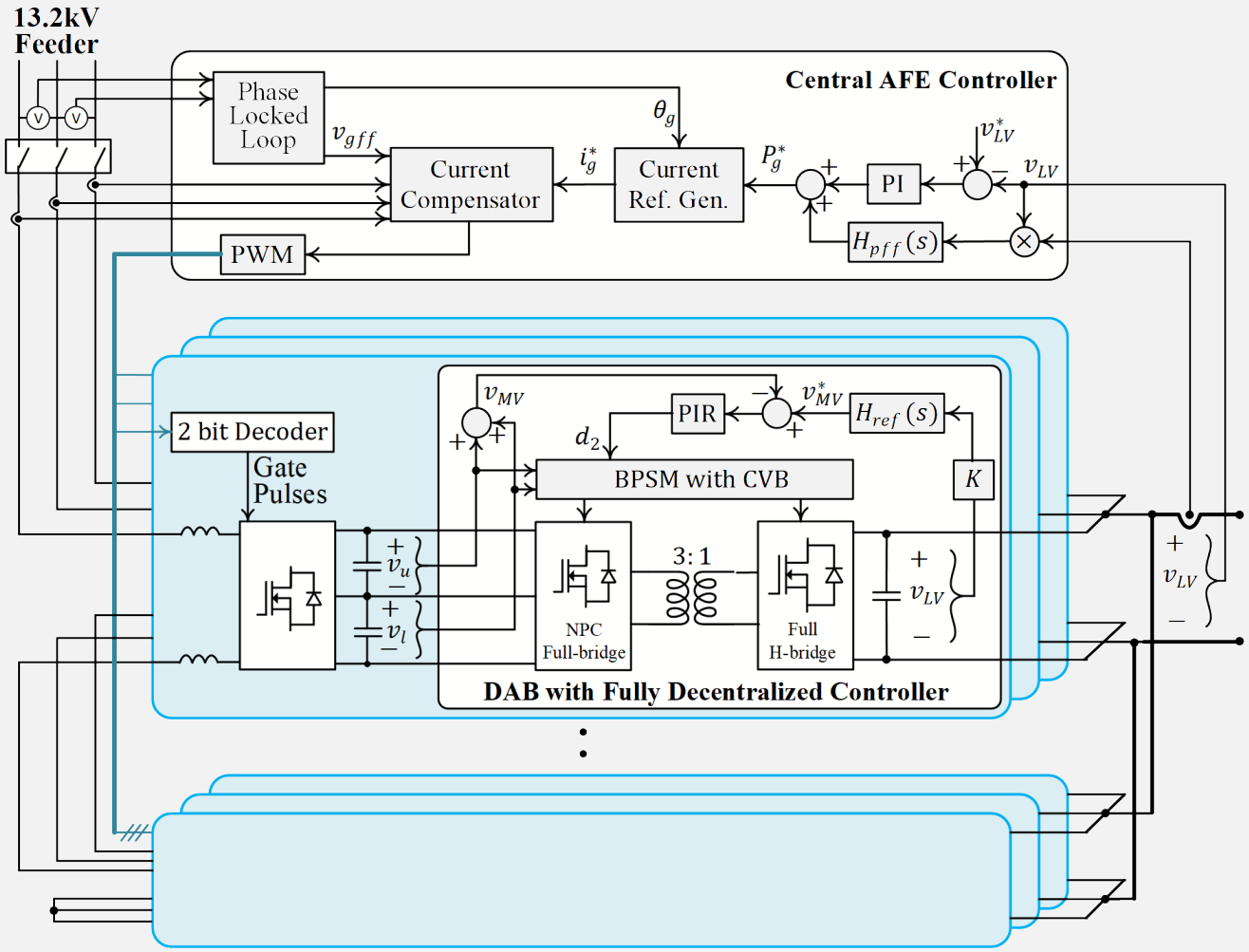
SST Architecture

- The SST connects to three-phase 13.2kV$_{LL}$ input and delivers 750V DC
- A total of 18 modules are arranged in 6 levels using input-series output-parallel configuration
- Each level is made up of three modules processing three-phase power on the input and delivering DC power at the output
- Each module consists of an active front end (AFE) and dual-active-bridge (DAB) isolated DC-DC stage



Design Approach & Control Architecture

- Each Dual active bridge (DAB) autonomously regulates its medium voltage (MV) bus, minimizing communication requirements
- Centralized controller for all AFEs with local protection and decoding
- Interleaved modulation of AFEs and low voltage (LV) side bridges of DABs
- DABs designed for sinusoidal power flow, minimizing storage requirements on MV DC capacitors
- Solid-state protection on MV and LV

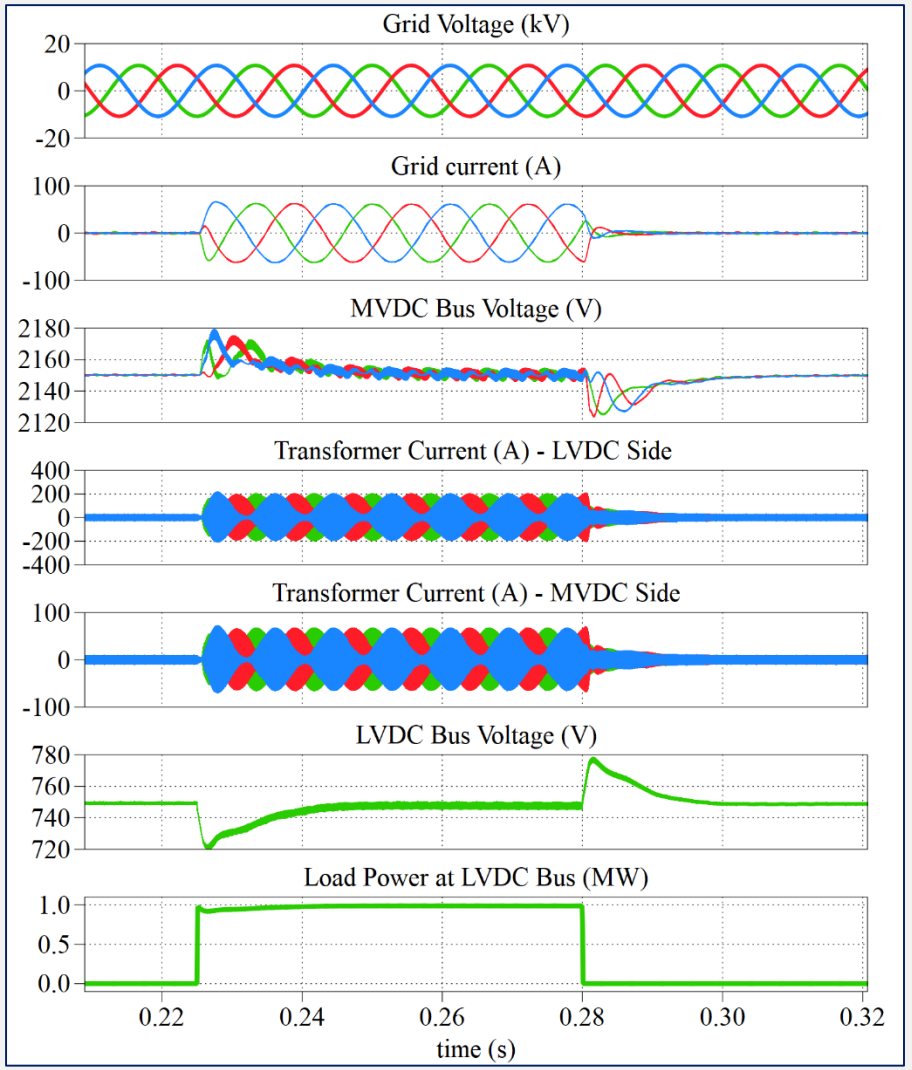


$H_{ref}(s)$ and $H_{pff}(s)$ are low-pass filters
PIR -- Proportional Resonant Integral Controller
BPSM with CVB -- Bidirectional phase-shift modulator with capacitor voltage balancing

Simulation Model for System Level Evaluation

No-load to full-load transition*

- System connects to 13.2kV feeder
- A step change in load causes a dip in the LV DC bus voltage
- Central AFE controller reacts by generating a grid current command
- DAB controller regulates the MVDC bus voltage to be proportional to the LVDC bus voltage feedback
- DAB controller uses a resonant compensation to minimize 2nd harmonic oscillation on the MV DC bus



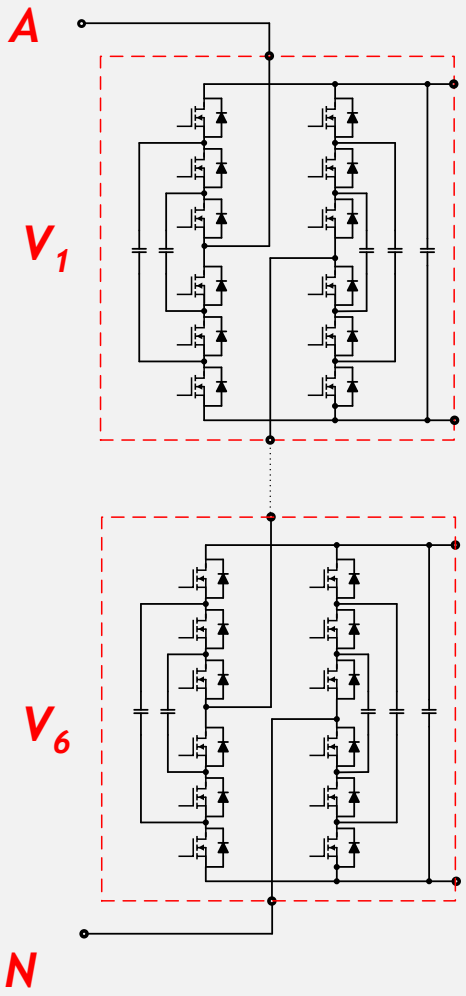
* Comprehensive simulations in Reviewer-Only slides

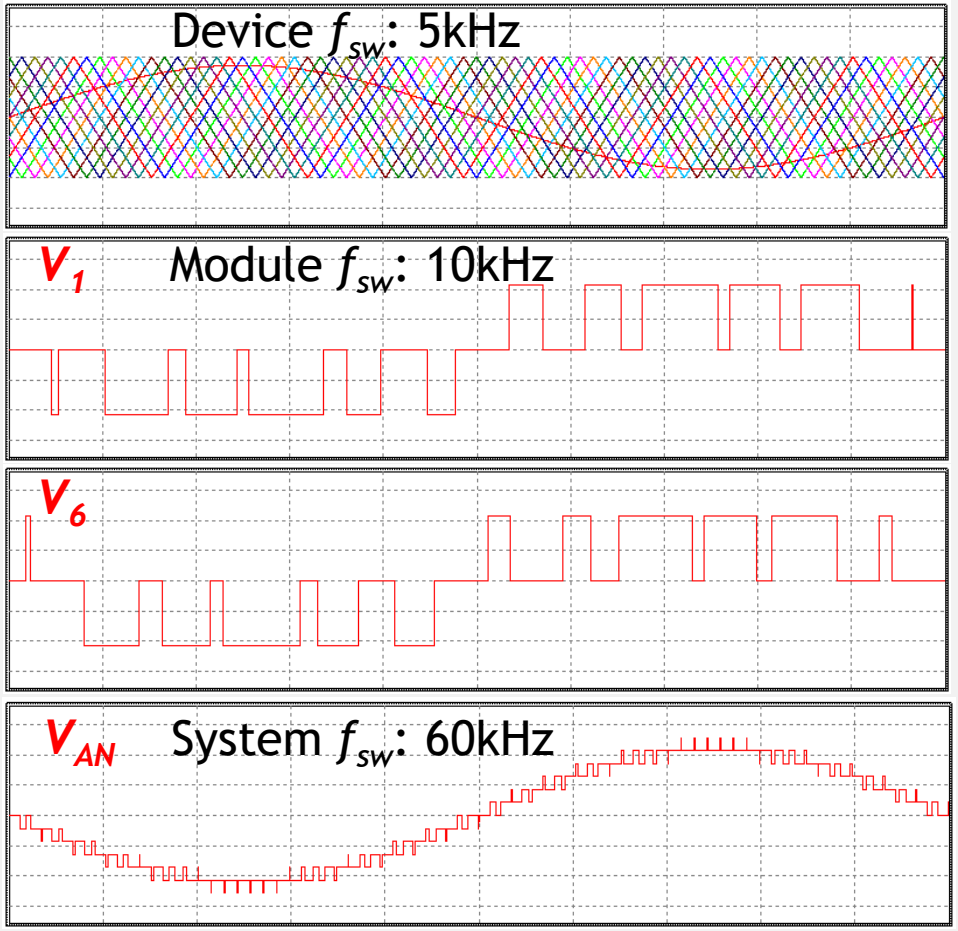
Active Front End (AFE)Topology

Cascaded-Flying-Capacitor Multilevel AFE

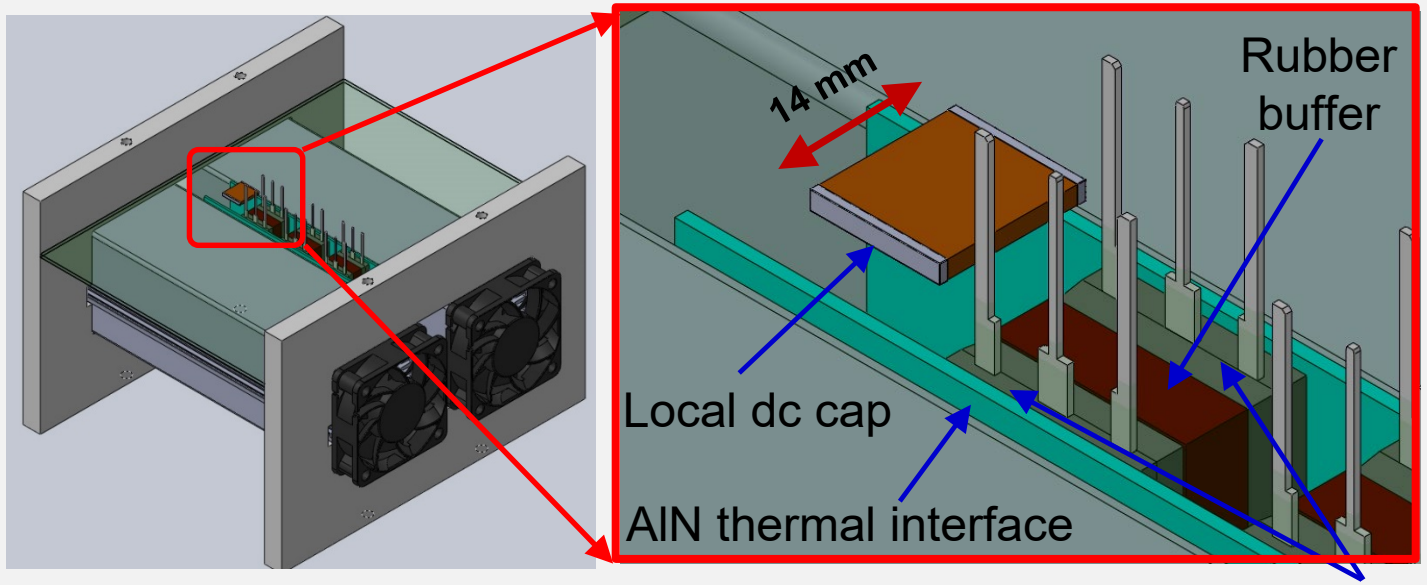
- Higher DC-link voltage (2.15 kV)
- Fewer isolation components
- Lower cost (1.2kV TO-247 SiC MOSFET*)
- 12X system versus device switching frequency
- Lower total harmonic distortion; smaller filter

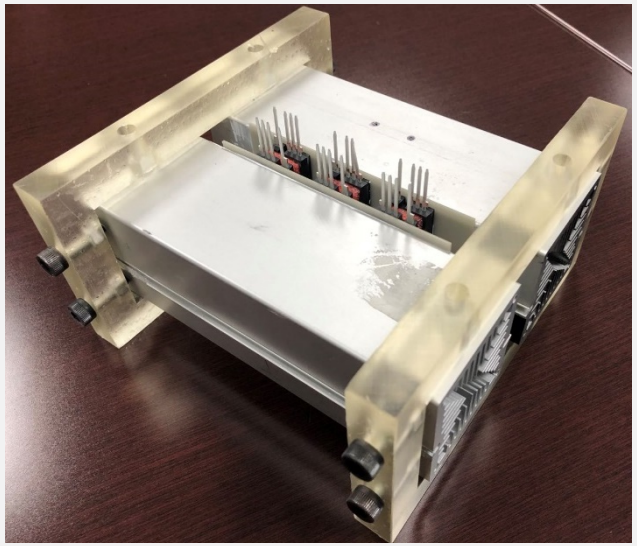
*SiC MOSFET – Silicon Carbide metal-oxide-semiconductor field-effect transistor





AFE Optimized Thermal and Loop Inductance





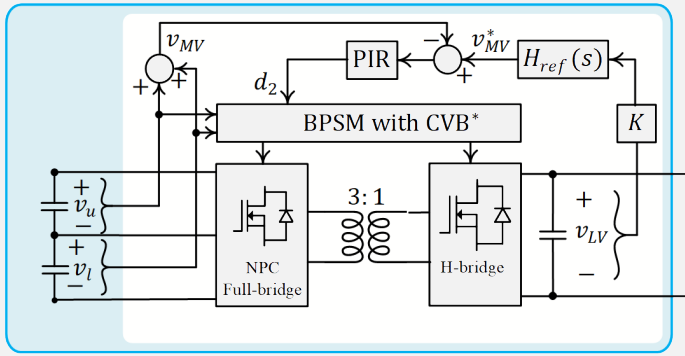
- Low cost TO-247 SiC MOSFETs
- Integrated cooling
- Optimized rubber buffer assembly
- Aluminum Nitride (AlN) thermal interface
- Minimum loop inductance

Half-bridge 1.2 kV SiC MOSFETs

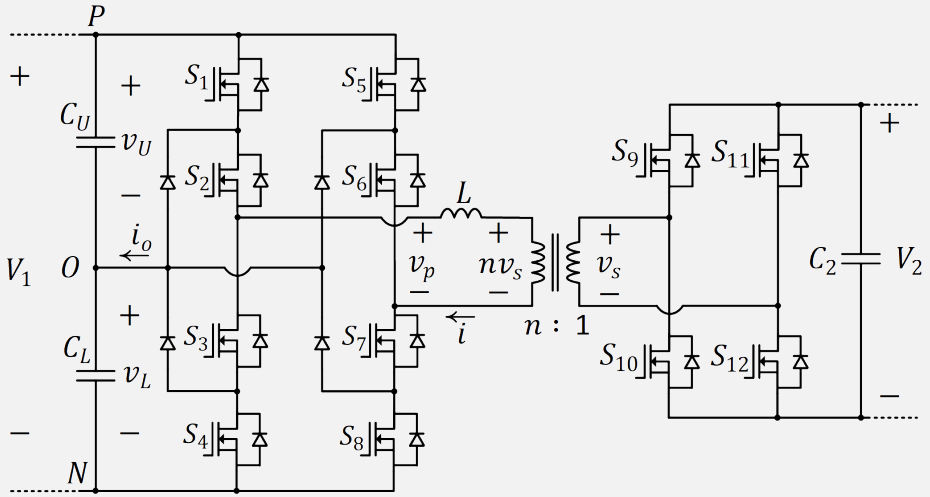
	AFE Module
Topology	Multilevel flying capacitor converter
f_{sw}	5 kHz
Device	C3M0016120D (16 mΩ / 1200V)
Flying Cap	68 nF

DAB Topology and Control

- All-SiC solution with 1700V modules on MV and 1200V modules on LV side
- Switching frequency of 20kHz, with module interleaving on the LV bus
- A proportional-integral-resonant (PIR) compensator eliminates 2nd harmonic oscillation on the MV DC bus
- A bidirectional phase-shift modulator (BPSM) with capacitor voltage balancing (CVB) generates the gate pulses for the primary and secondary bridges of the DAB



Dual Active Bridge (DAB) with Decentralized control



Medium Voltage Side: Neutral Point Clamped (NPC) Full-Bridge

Low Voltage Side: H-Bridge

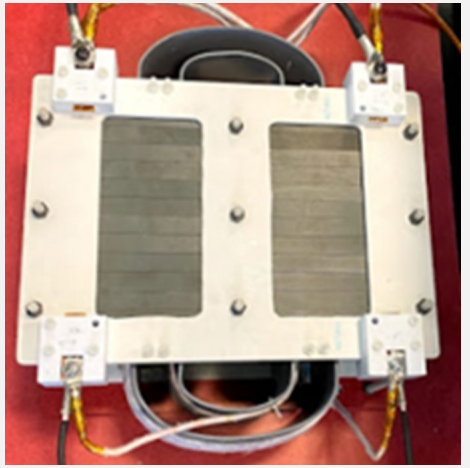
Transformer Design

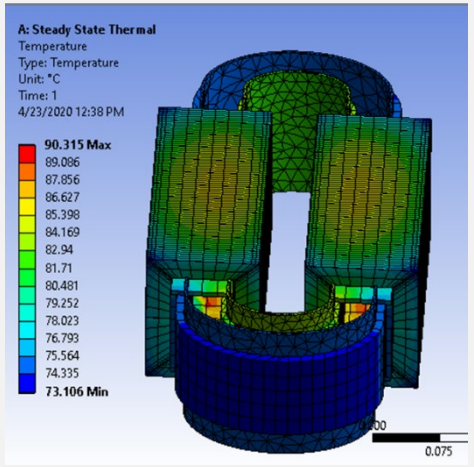
Design Challenges

- Application requires partial discharge inception voltage to exceed 40kV
- Thermal design for natural air flow cooling
- Simple construction allowing repeatable results
- Controlled leakage inductance

Design Approach

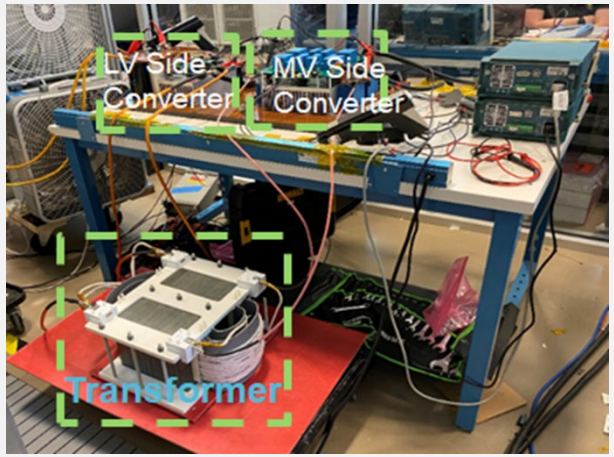
- Rely on winding separation in air to meet isolation requirements; reinforced isolation between windings and core
- Compatible with transformer insertion in oil
- Relatively low flux in ferrite distributes heat and ensures operation in linear range

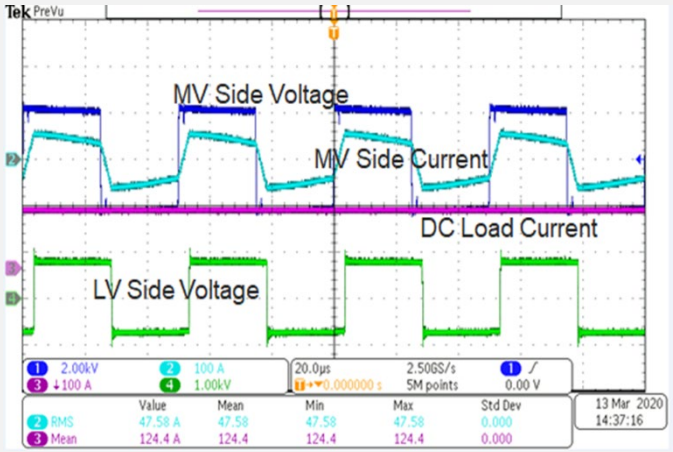


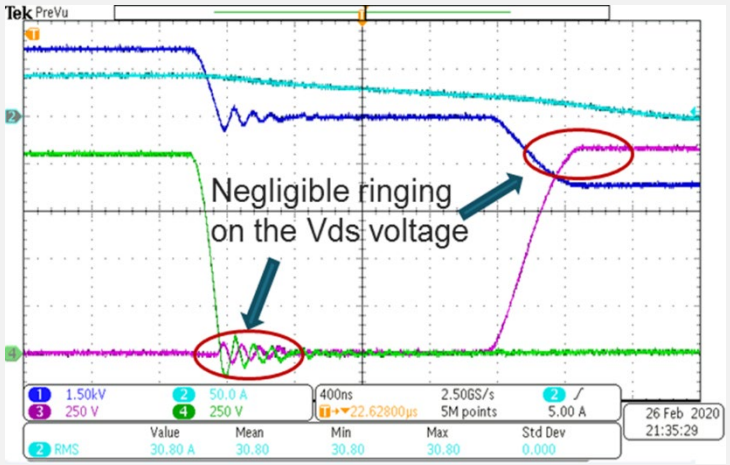


Parameter	Value
Primary/Secondary Voltage	±2,150V / ±750 V
Frequency	20 kHz square wave
Average (Peak) Power	83 (167) kW
Primary/Secondary current	63Arms / 180Arms
Transformer efficiency	> 99%
Primary leakage inductance	137 uH
Magnetizing inductance	13.4 mH
Parasitic capacitance	116 pF

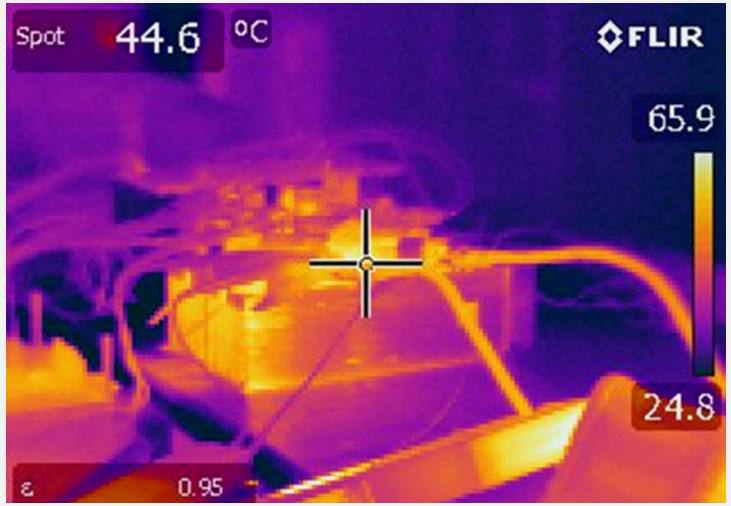
DAB Stage Testing



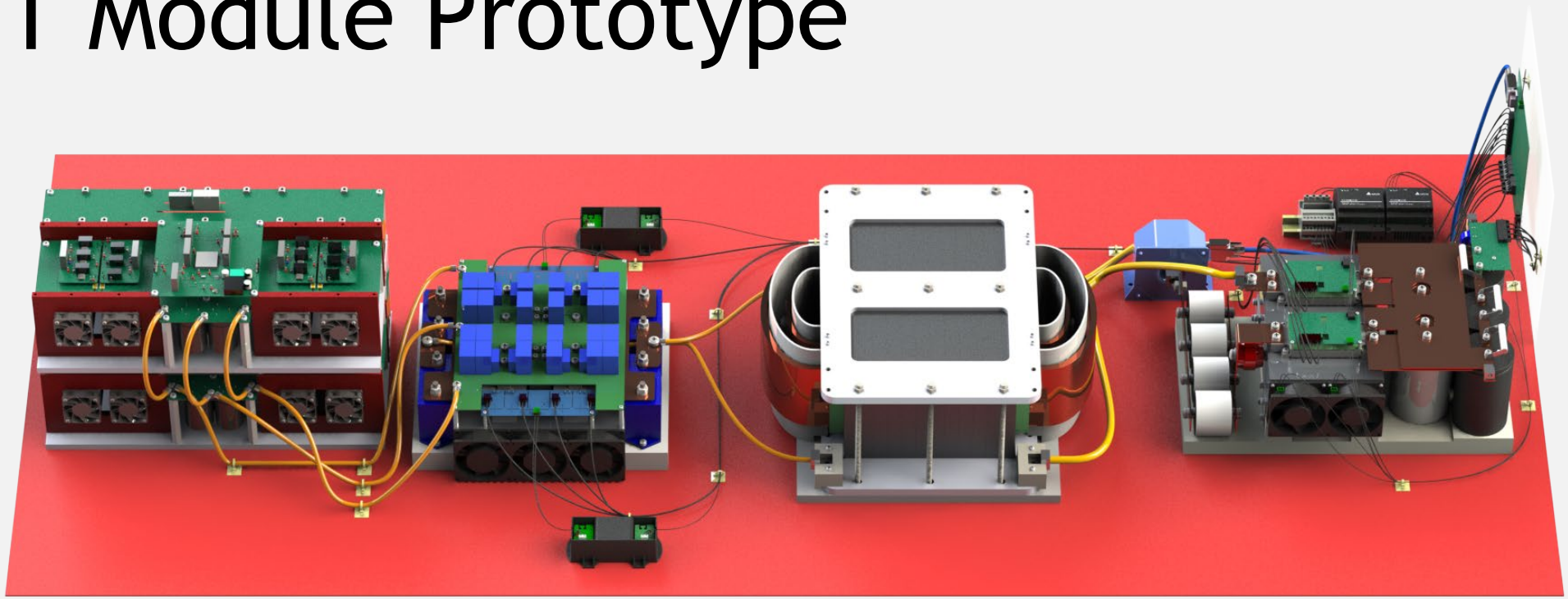


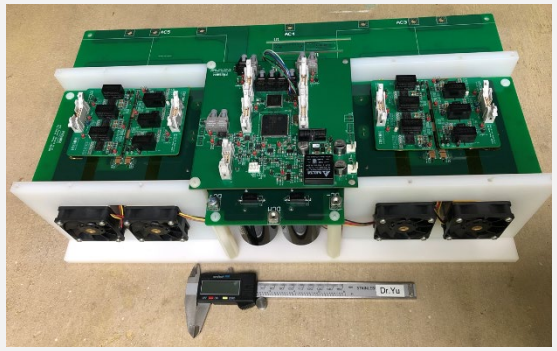


- DAB stage tested at 95 kW in open loop; efficiency measured at 98.9%, all devices soft-switched
- Hotspot within 70 degree under long-term operation
- Low voltage overshoot on device drain-to-source voltage

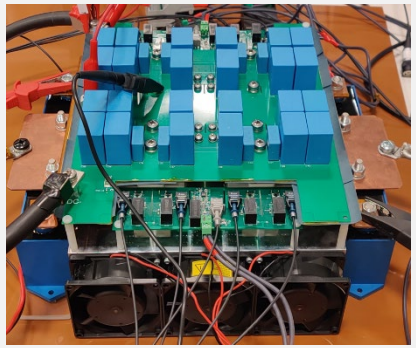


SST Module Prototype

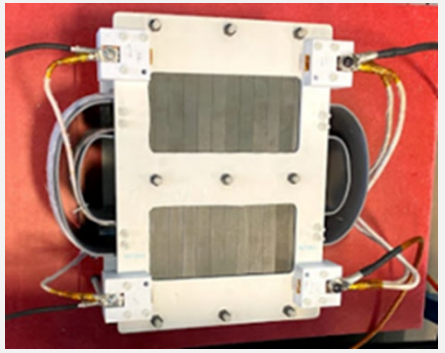




Active front-end



DAB MV side

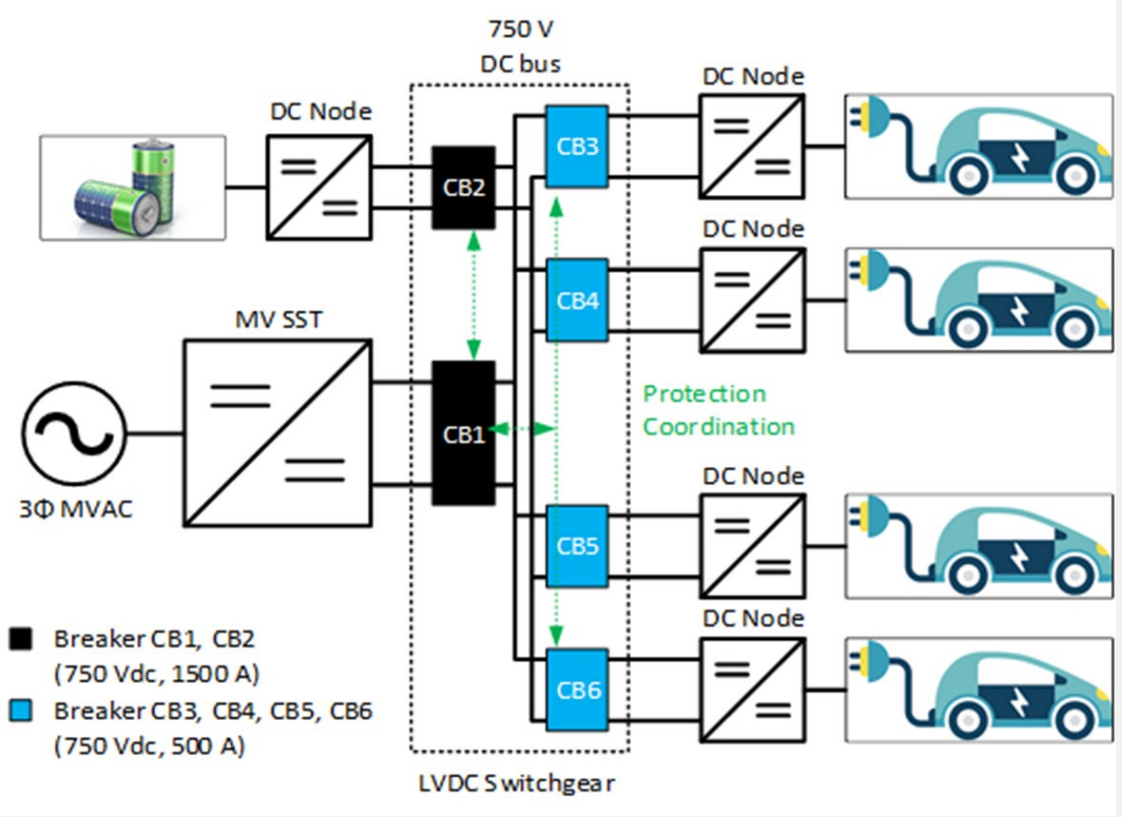


Transformer

DAB LV side

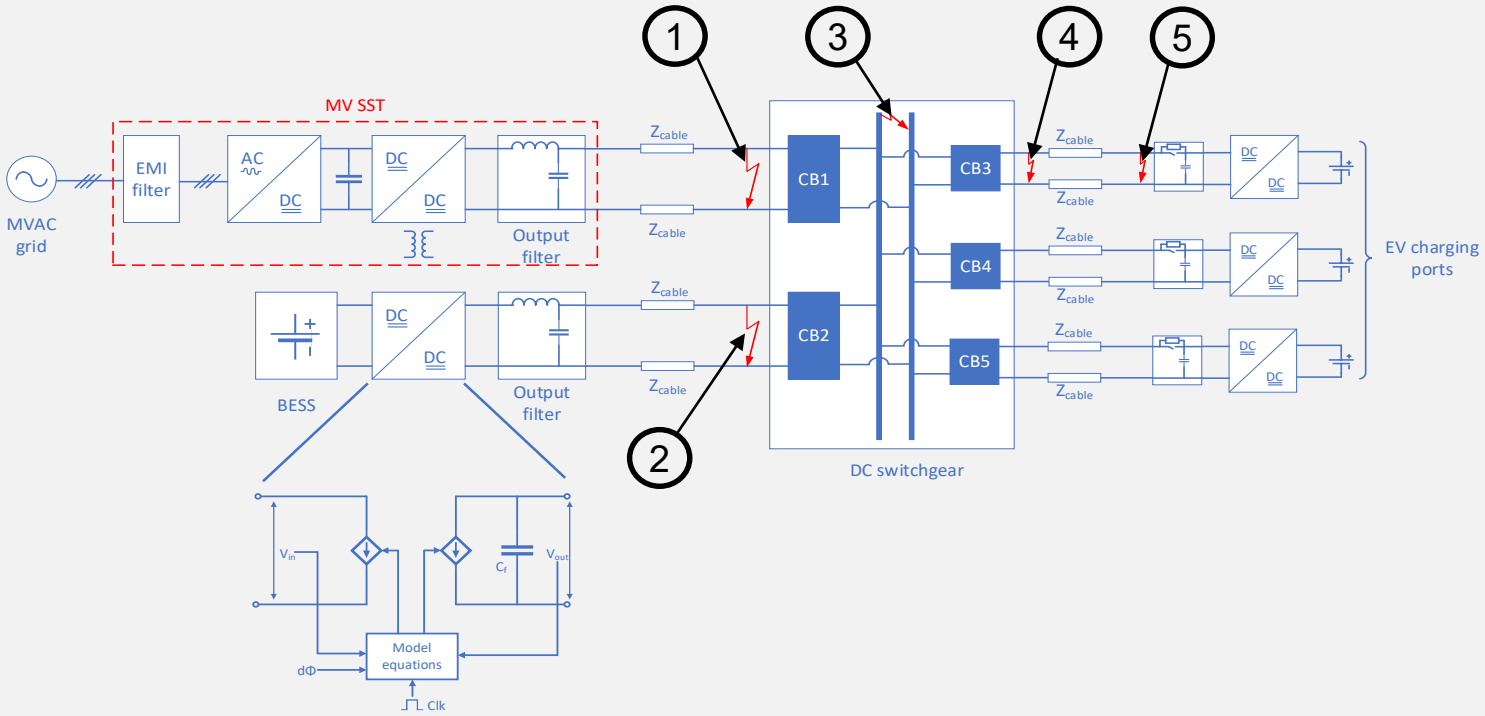
DC distribution with solid-state protection

- High penetration of power converters requires fast system protection components and algorithms to be developed
- Commercially available breaker technology is not fast enough to guarantee protection coordination
- We are developing two classes of Solid State Circuit Breakers (1500 A and 500 A) and fast fault detection and coordination algorithms



System study and protection coordination

- Minimum effective inductance for a downstream fault estimated to be < 5 µH
- Consequently, maximum fault di/dt is 280-300 A/µs
- di/dt based mixed signal trip unit is required to trip breaker within 8-9 µs and ensure selectivity

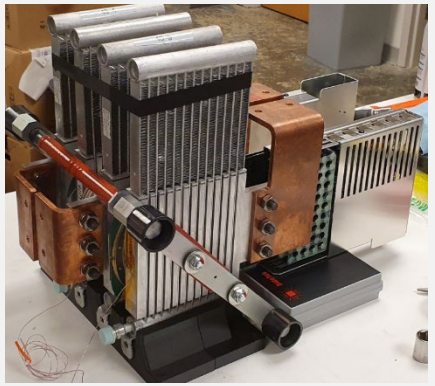


Solid State Breakers Design

Solid State Circuit Breaker Technology

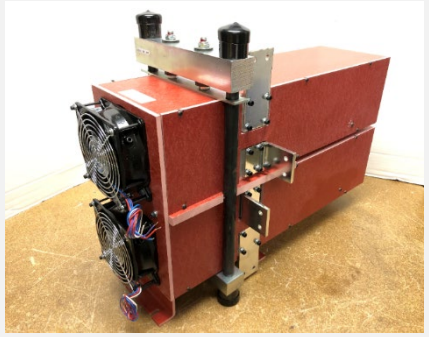
- Ultra-fast Mixed Signal Fault Detection for high di/dt
- Low conduction loss RB-IGCT for high efficiency and fast interruption
- Advanced 2-phase cooling for 1500 A breaker for high power density
- Forced air cooling for 500 A unidirectional breaker

RB-IGCTs + 2-phase cooling



1500A SSCB - Bidirectional

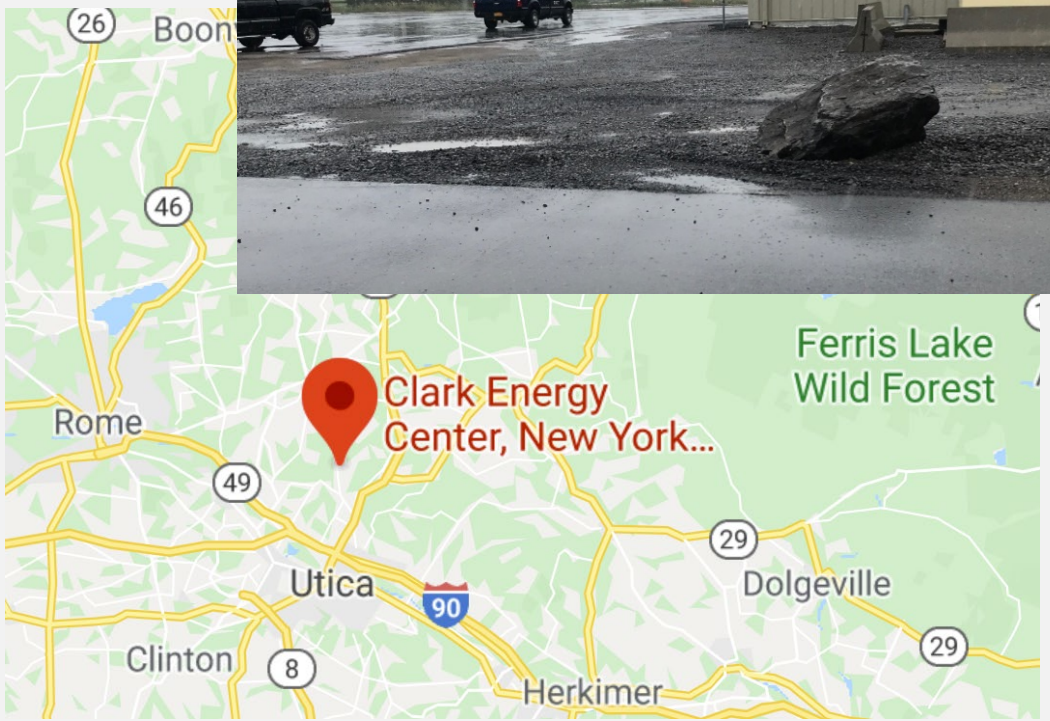
RB-IGCTs + forced air



500A SSCB - Unidirectional

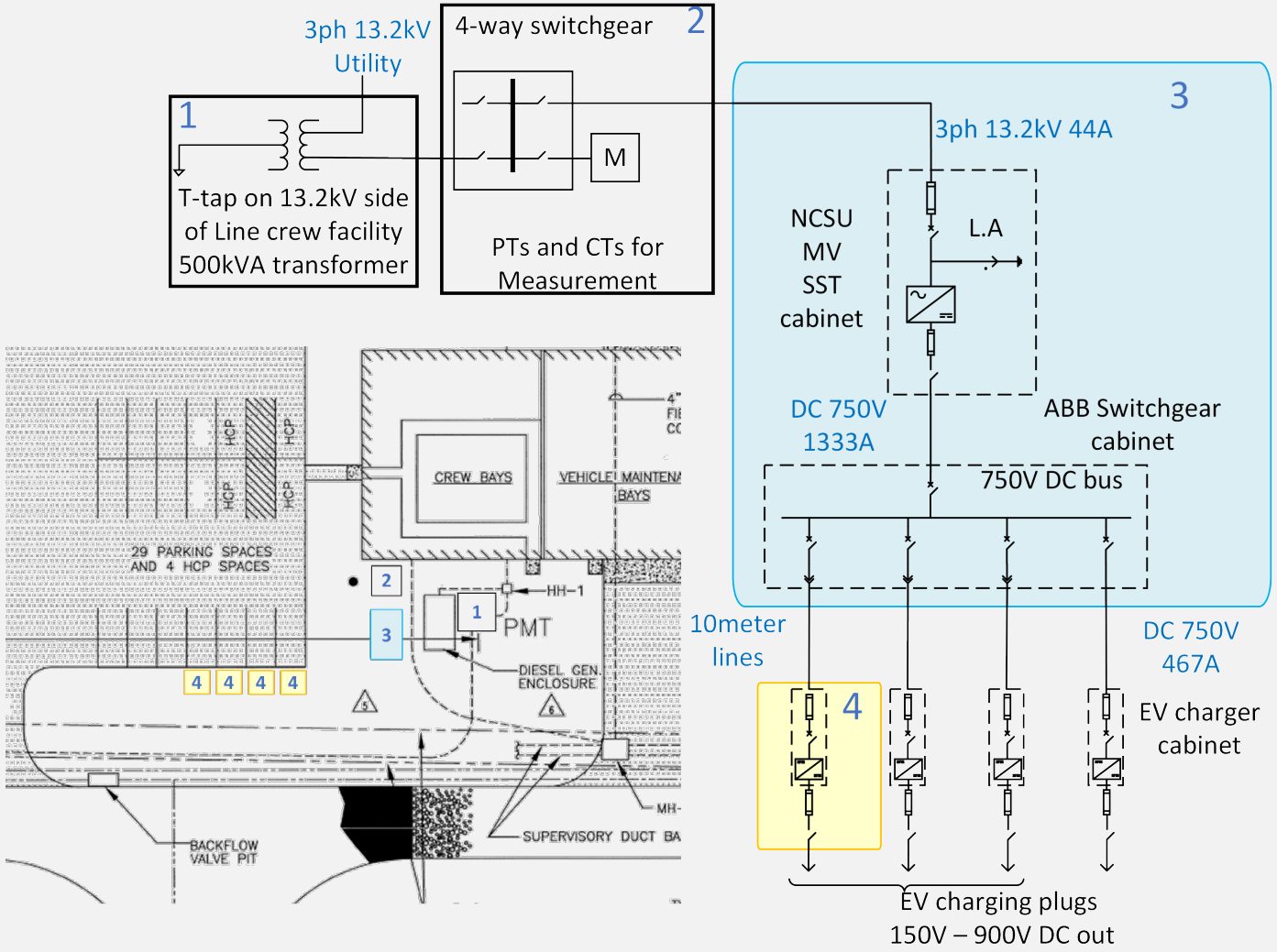
Site Selection

- NYPA is a self-permitting entity; NYPA identified demonstration site at a facility in Marcy, NY
- Utilizes an existing 13.2 kV connection
- Site is in a secure facility where all personnel are trained to handle high voltage systems
- NYPA identified local contractor to begin generating engineering drawings



Site Layout

1. XFC Station connects to a T-tap on the 13.2kV side of a line crew facility 500kVA transformer
2. New 4-way switchgear will allow for isolation of the XFC from the utility
3. XFC SST and MV and LV solid state protection will be housed in a customized 20-foot shipping container
4. Four enclosures house DC nodes



Responses to Previous Year Reviewers' Comments

- This is the first year that the project has been reviewed

Collaboration & Coordination with Other Institutions

- **NCSU:** SST, DC Node (DC/DC converter) development; XFC system integration.
- **ABB:** development and testing of the solid-state breakers and system protection scheme. Help identify and source near-commercial DC/DC stage
- **NYPA:** system deployment and demonstration.

Remaining Challenges and Barriers

SST Stage:

Complete Assembly and testing of SST; delays due to the contracting delays, component sourcing and covid-19 pandemic.

DC Protection:

Testing of breaker units for short circuit with very high di/dt typical of the proposed system architecture. Testing of coordination between upstream and downstream breakers with high di/dt short circuit fault scenarios.

Site Preparation:

Finalize detailed engineering drawings.

Proposed Future Work

Key Challenges

- Design of the SST stage, meeting key safety requirements
- Design and coordination of solid state protection
- Procuring vehicle loads capable of stressing the charger system

Future Work

- Demonstrate SST and DC Nodes
- Demonstrate solid state breakers and protection coordination
- System Integration

Any proposed future work is subject to change based on funding levels

Summary

- Team on track to demonstrate a 1MVA XFC station with
  - A MV SST that connects directly to distribution grid
  - A shared DC bus that allows for local energy management to alleviate stress on the grid
- Three year project plan:
  - 2020: Component Validation
  - 2021: System validation
  - 2022: System Deployment and Data Collection

Technical Backup Slides

DAB Control

- The voltage reference is generated based on LVDC bus feedback; a first order low-pass-filter (LPF) is used as

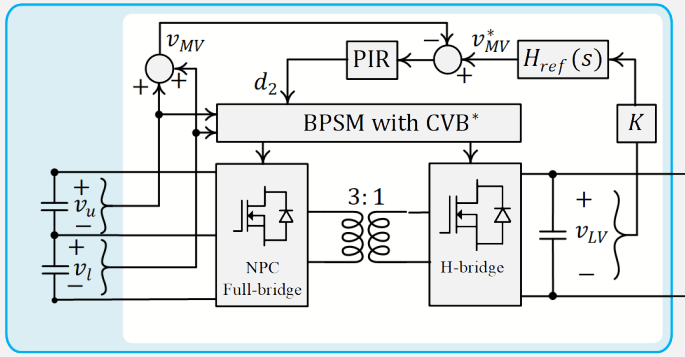
$$v_{MV}^{*}(s) = H_{ref}(s) \times K \times v_{LV}(s)$$

$$H_{ref}(s) = \frac{\omega_{c,ref}}{s + \omega_{c,ref}};\ K = 2150/750$$

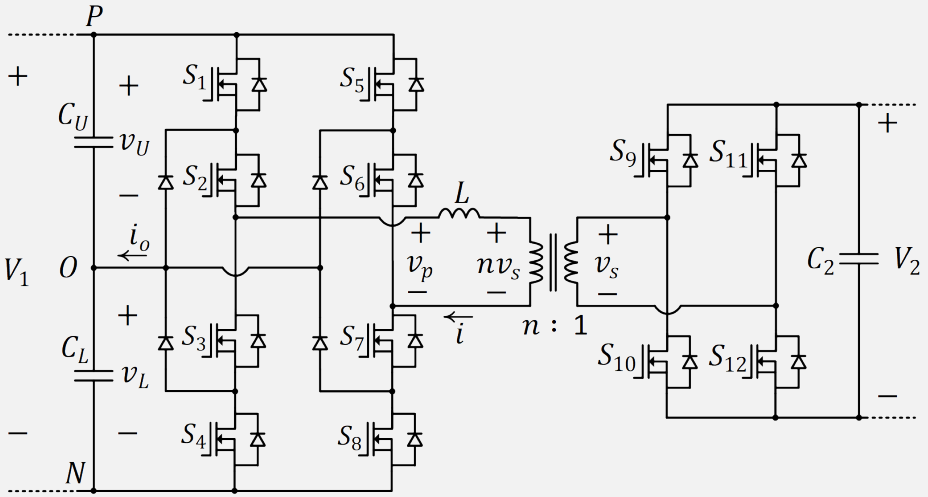
- A proportional-integral-resonant (PIR) compensator eliminates the 2nd harmonic oscillation on the MVDC bus

$$F_{PIR}(s) = K_{pmv}\left(1 + \frac{1}{\tau_{mv}s} + \frac{1}{\tau_{rmv}} \times \frac{\omega_{rb}}{s^2 + \omega_{rb}s + \omega_2^2}\right)$$

- A bidirectional phase-shift modulator (BPSM) with capacitor voltage balancing (CVB) is used to generate the gate pulses for the primary and secondary bridges of the DAB



Dual Active Bridge (DAB) with Decentralized control

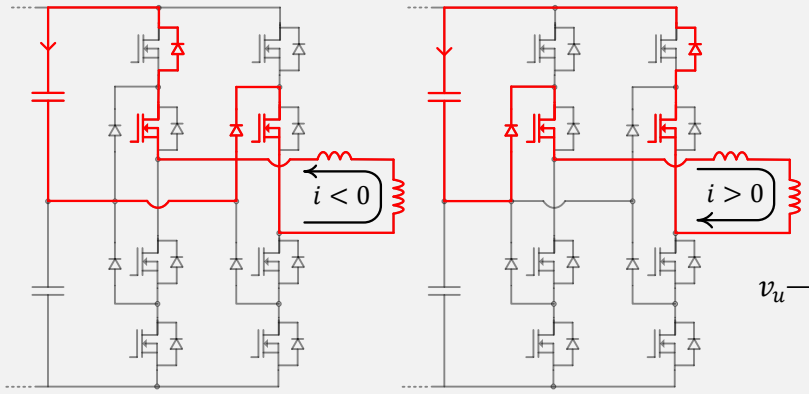


Medium Voltage Side: Neutral Point Clamped (NPC) Full-Bridge

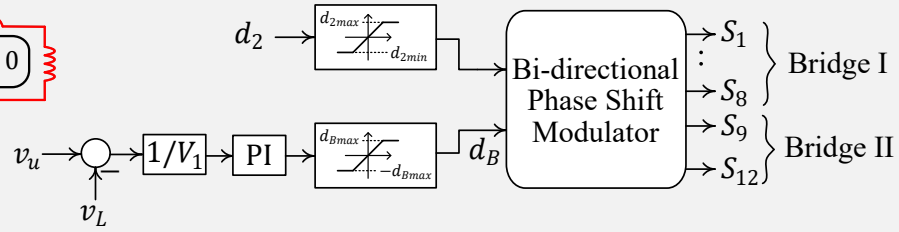
Low Voltage Side: H-Bridge

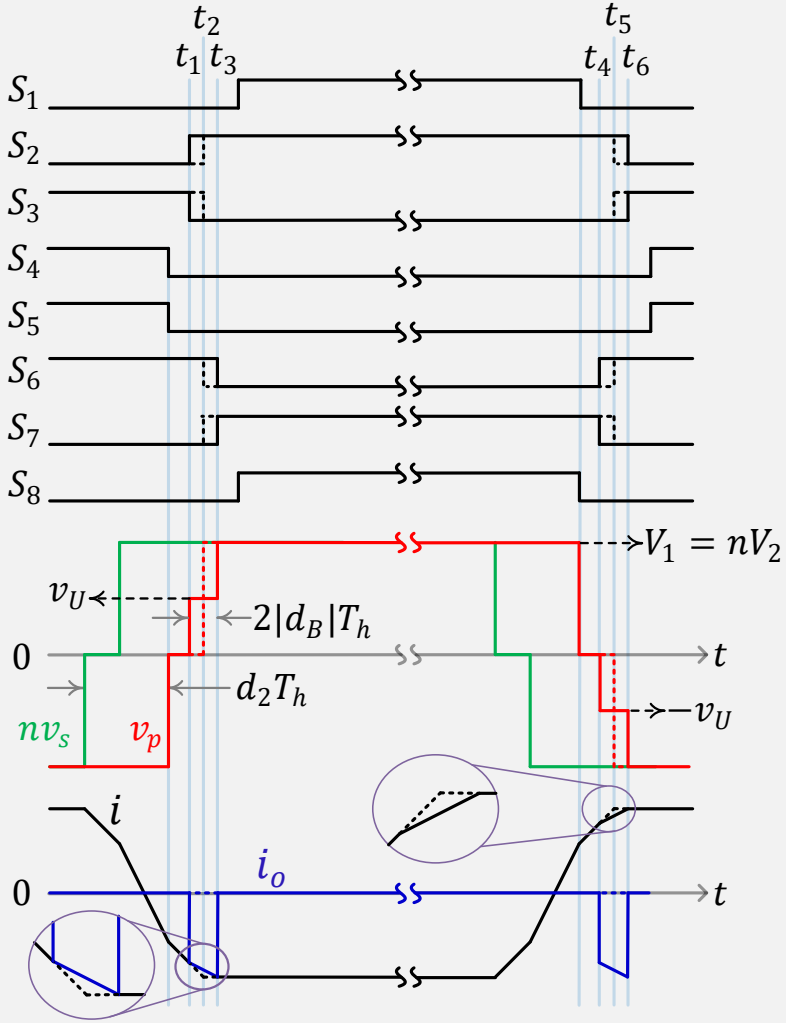
DAB Control: Bidirectional Phase-Shift Modulation with Capacitor Voltage Balancing

- Capacitor voltage balancing is achieved independent of power flow direction
- Modulator does not need to actively select between small voltage vectors; neutral current generated automatically by power stage
- No voltage offset introduced across transformer terminal
- Only one switching transition within one switching period



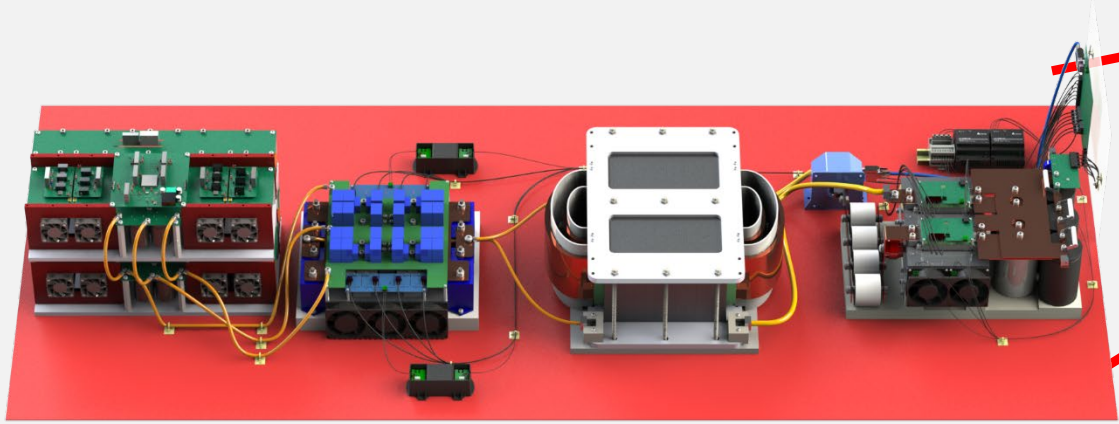
Charging the upper capacitor irrespective of direction of transformer current

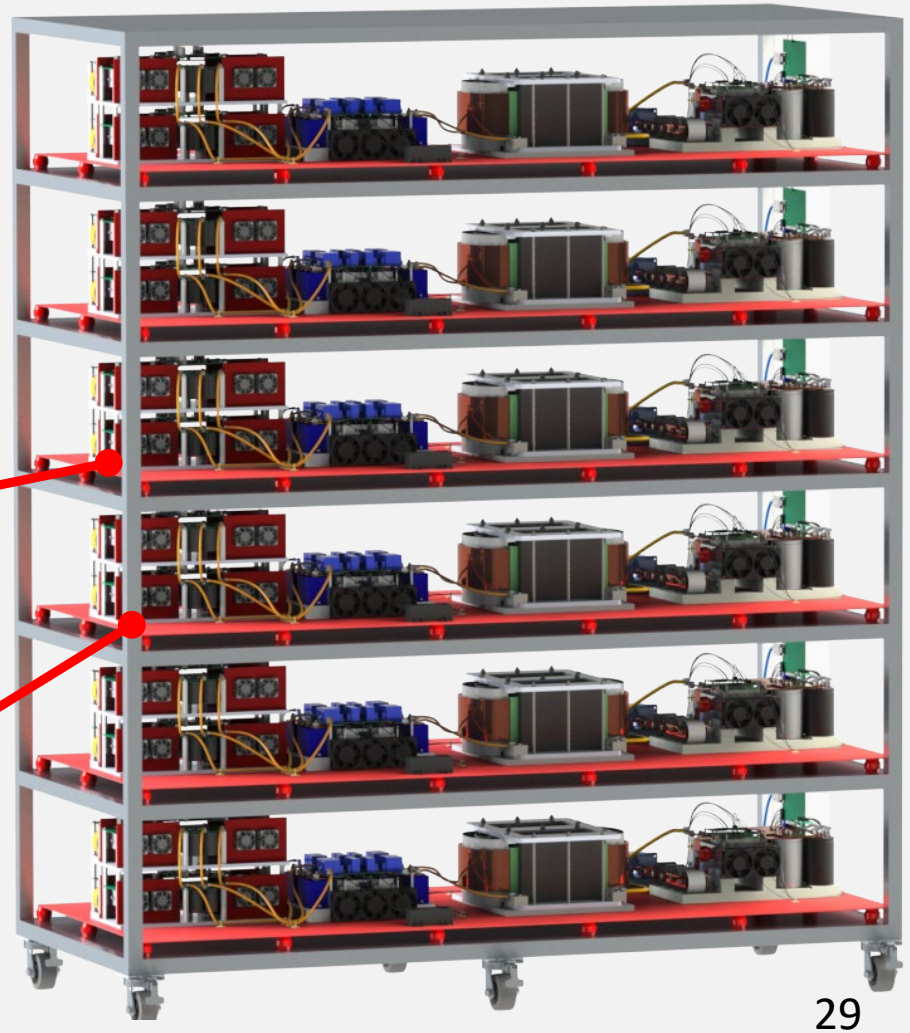




Lab Implementation of initial SST Prototype

- Initial SST prototype will be tested at 500kVA in the NCSU lab using resistive loads
- System will be stacked on racks while preserving thermal and electrical isolation between individual modules
- System-level thermal design for the shipping container enclosure is in process

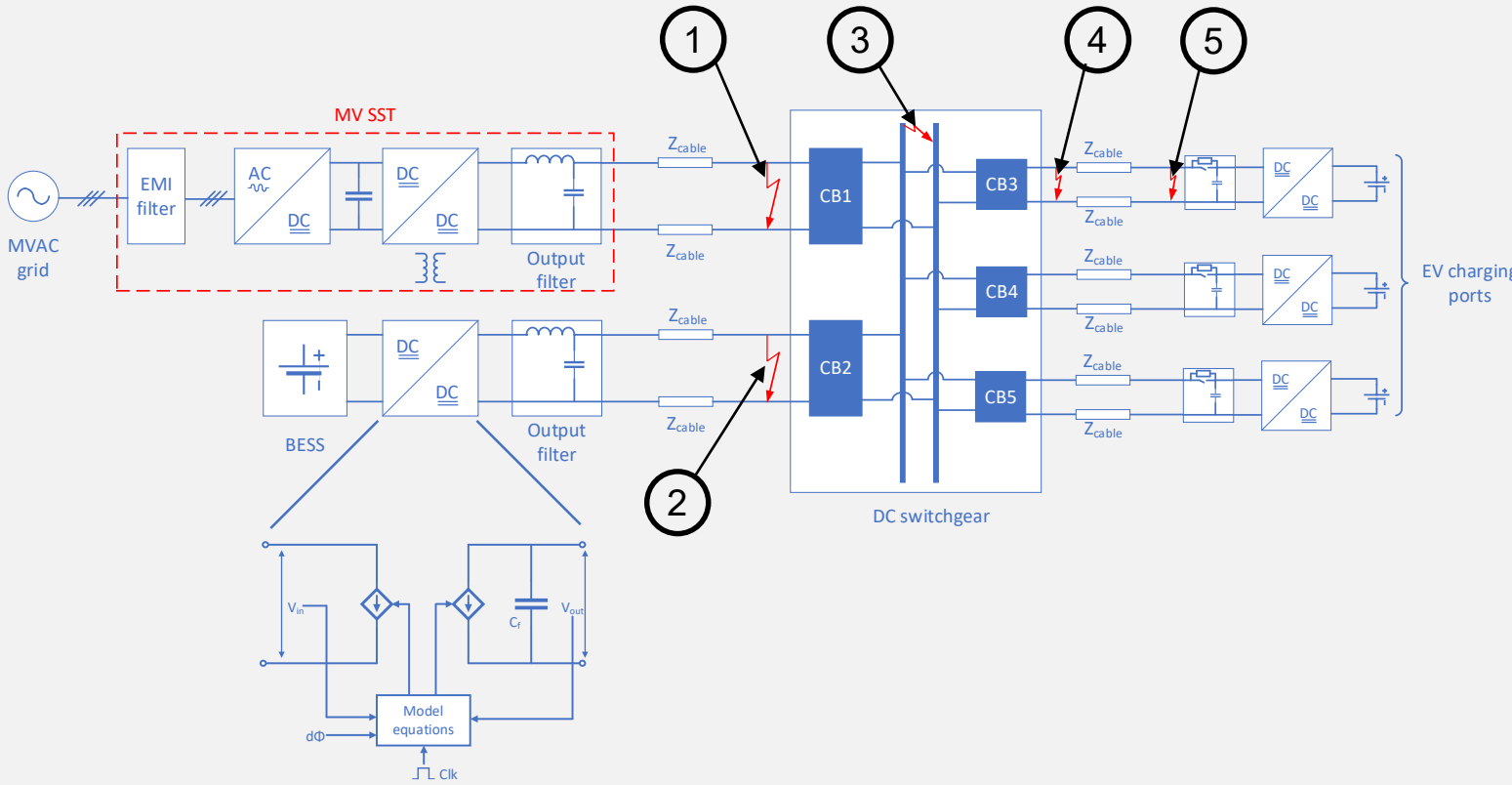




System study and protection coordination

Fault scenarios under investigation (sample):

1) Fault at the output of the SST
2) Fault at the output of the BESS DC-DC converter
3) Fault at the DC bus (within the switchgear cabinet)
4) Fault on one of the charger branch, just after CB3 breaker (high di/dt fault)
5) Fault on one of the charger branch, near the input of the charger DC-DC converter (lower di/dt fault compared to 4)



1 MW extreme fast charging system under study

Protection Coordination - Example

Fault location 4 – demonstration of high availability

- Worst case for fault di/dt : ~280A/µs*
- Initial current in CB1 : ~1500A
- Initial current in CB3 : ~500A
- Peak fault current in CB3 : 2600A
- Time to trip : 8.2µs
- Negative di/dt in CB4 and CB5 is also reflected in the positive fault di/dt in CB3